Design aspects of a wideband RF Front-end for an Adaptable Radio Platform

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Abstract - *The continually increasing demand for high data rates, low-latency and high user density has contributed to the rapid evolution of radio standards, generating a need for flexible, high-performance platforms that can dynamically access different parts of the radio spectrum for a variety of applications and operations. A software-defined radio (SDR) platform provides an elegant solution by offering functional flexibility and application adaptability through reconfigurable hardware. Realisation of a compact, multi-board, SDR platform necessitates the use of high-density interconnect (HDI) implementation.*

This paper introduces an RFSoC (RF System-on-Chip)-based SDR platform realised in a dual-slot PCIe form-factor. The design methodology and challenges in utilising high-density array connectors, typically used for high-speed digital interconnections, for routing RF signals in a multi-board design are presented.

1. Introduction

Figure 1 illustrates a traditional heterodyne transceiver architecture, wherein the baseband-to-RF signal (and vice versa) conversion, amplification, and signal conditioning is performed in the analogue domain using dedicated, fixed hardware. As the RF hardware is designed for specific frequency bands and applications, it limits the architecture's flexibility and adaptability.

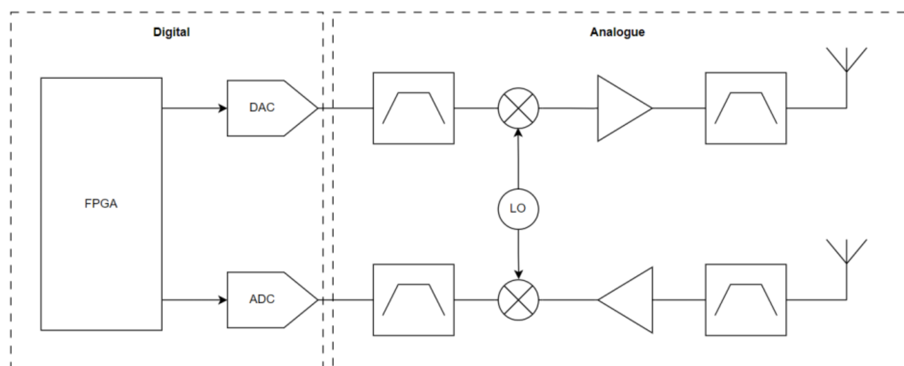


Figure 1 A traditional RF front-end architecture where a large portion of the signal processing is performed in the analogue domain.

Advances in high-speed data converters, embedded processor units and digital signal processing techniques have led to the advent of SDR. A large section of the signal processing chain, previously constrained to the analogue domain, can now be implemented in the digital domain. The high-speed data converters, capable of sampling at gigahertz (GHz) data rates, enable digitisation and signal generation directly at the RF frequencies, thus, eliminating or reducing the need for analogue mixing stage(s). The frequency conversion can, instead, be performed in the digital domain, as shown in Figure 2. This is known as a Direct RF-sampling architecture because the sampling is being performed directly at the RF frequencies. Additional signal processing

techniques, such as digital pre-distortion (DPD), crest-factor reduction (CFR) and filtering can also be performed in the digital domain. This contributes to an improvement in the system linearity performance as well as a reduction in the external analogue circuitry required.

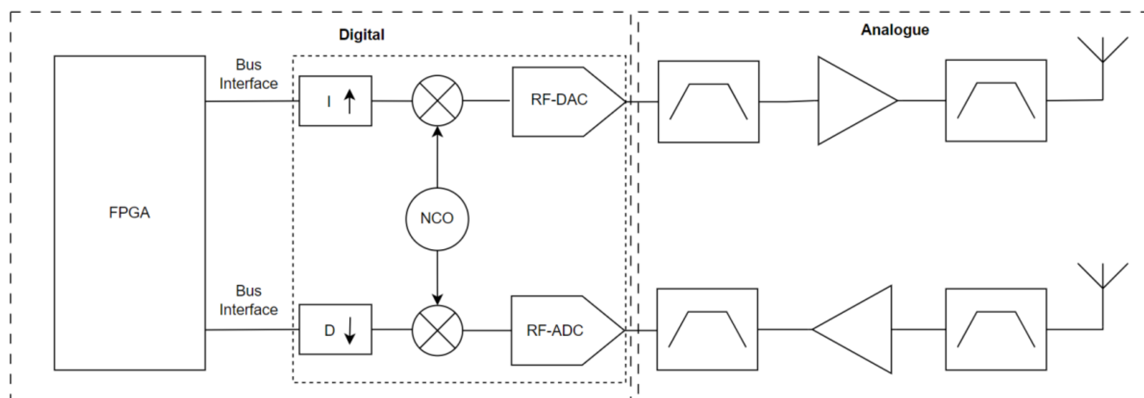


Figure 2 A generic SDR architecture wherein a large section of the signal processing is performed in the analogue domain.

As a large part of the functionality is implemented in the digital domain, an SDR platform can be reconfigured dynamically to handle diverse frequency allocations and standards, making it flexible and adaptable. This is favourable in modern transceiver systems where the radio standards are evolving rapidly. In this paper, an RFSoC-based SDR platform, implemented in a PCIe form factor, is introduced in Section 2. An overview of its advantages in terms of reconfigurability and adaptability is provided.

Routing the RF signals from the RFSoC device to the RFFE board via multiple connectors, whilst maintaining the return loss and crosstalk performance, is a key design challenge. In this work, high-density field array connectors from Samtec have been exploited to achieve these multi-board transitions. These connectors have traditionally been used in high-speed digital signal interconnections. The work done in designing the connector-to-board transitions for these connectors to route analogue RF signals up to 6 GHz has been presented in Section 3.

2. RFSoC-based SDR Platform

A top-level architecture of Xilinx AMD's Zynq UltraScale+ RFSoC device is presented in Figure 3. An RFSoC provides an integrated solution for an SDR platform by incorporating high sampling rate (giga samples per second sampling rate) data converters, FPGA programmable logic (PL), ARM-Cortex processing systems (PS), high-speed serial links (GTY) and hardened DSP blocks (for example, soft-decision forward error correction) directly on-chip. The 3rd generation (Gen 3) of AMD's RFSoC integrates 8 RF digital-to-analogue converters (DACs) and 8 RF analogue-to-digital converters (ADCs), each capable of sampling at 9.85 GSps and 4.915 GSps, respectively, in a 35 mm x 35 mm package. The integrated nature enables a compact physical realisation of the system.

In this work, a Gen 3 RFSoC has been utilised to design an SDR platform (ASTRO^{TM}) with an 8-lane PCIe carrier card, as illustrated in Figure 4. The RF Front-end (RFFE) card incorporates 8 transmit 8 receive (8T8R) channels and is designed to operate in the 5G NR N78 and N77u bands (3.4-4.2 GHz). However, the flexible and reconfigurable nature of the ASTRO^{TM} SDR platform allows for the RFFE board to be a plug-and-play module that can be swapped depending on the application of interest.

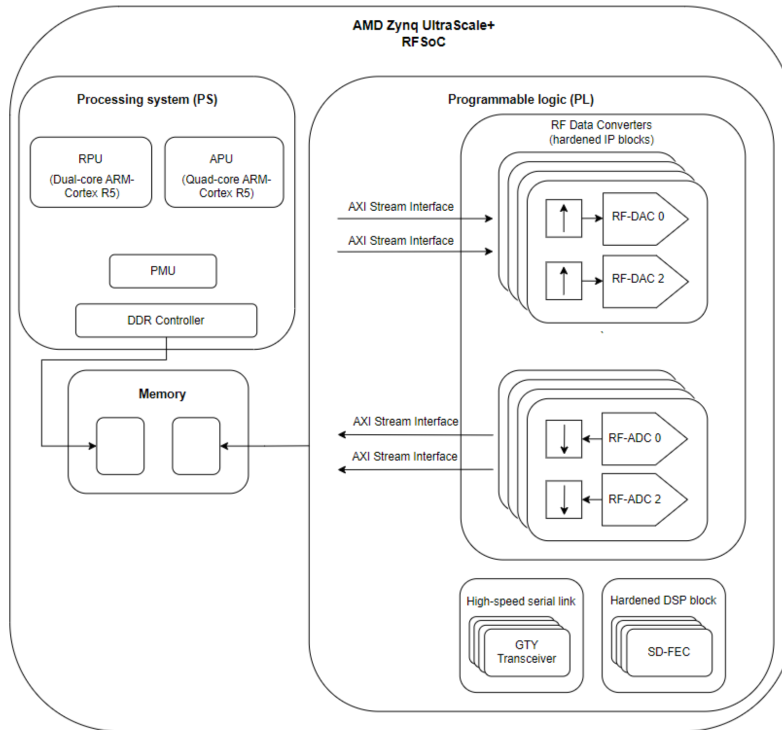


Figure 3 An overview RFSoC as an integrated solution [2]

The GSps sampling rates imply that the RF data converters can generate and capture large bandwidths from 0 Hz to $f_S/2$, where f_S is the sampling frequency. Sub-6 GHz applications such as cellular networks (4G LTE, 5G NR FR-1) and radar sensing can benefit from this architecture by reducing the required external analogue circuitry and the overall complexity. In addition, due to its wideband capability, an RFSoC can support multi-band operation on a single channel. For frequencies greater than the RFSoC's analogue bandwidth of 6 GHz, an external mixing stage would be required to translate the frequencies down to the sub-6 GHz band.

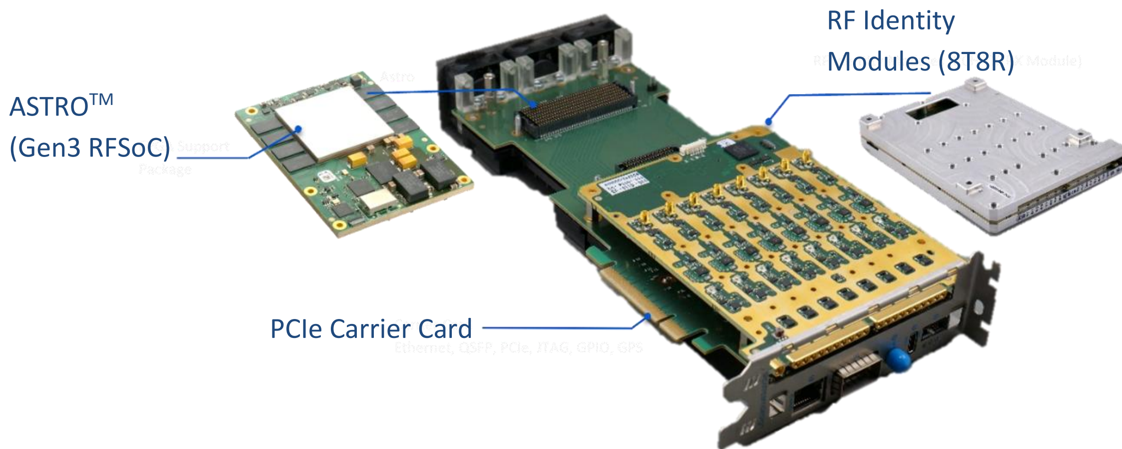


Figure 4 Slipstream's SDR platform comprising of ASTRO™ that houses a Gen 3 RFSoC, an 8T8R channel RFFE in a dual-slot PCIe form-factor.

A wideband and reconfigurable analogue front-end is desired to realise a fully flexible and reconfigurable SDR platform. The wideband RFFE designed in this work incorporates an on-board FPGA that can be configured by the RFSoC device via I2C protocol. The FPGA enables device level and channel level control of the RFFE, thus, facilitating dynamic gain control over

the channels. In addition, the RF channels can be selectively turned on/off to reduce power consumption and improve the system performance. The incorporation of an FPGA with a BGA footprint and device-level control further enhances the need for HDI implementation. The HDI implementation is discussed in detail in Section 3.

The RFFE is a wideband, low-power solution. To realise a complete SDR platform, a reconfigurable power amplifier and a reconfigurable front-end filter are required. This can be achieved by employing electronically-tuneable filters and a digitally-controllable power amplifier. By exploiting a dual-input LMBA architecture along with the DPD functionality offered by the RFSoC, a reconfigurable power amplifier can be realised. Similarly, tuneable filters can be achieved by using varactor diodes or FETs for planar filters or digitally-controlled motors for coaxial cavity filters.

The following section discusses in detail the design methodology and challenges encountered in the high-density implementation of a compact sub-system as described above.

3. High-Density Interconnect Implementation

High component density and fine-pitch components are required to facilitate 8T8R channels in a compact form factor. To achieve the desired functionality, a high layer-count PCB with fine track widths and microvias is required. Routing the 8T8R channels from the RFSoC board, through the PCIe carrier card, to the RFFE board whilst maintaining high isolation, good return loss and minimum insertion loss within the required compact form factor is challenging. High-density field array connectors which are traditionally used for routing high-speed digital signals, were exploited to route the RF signals through multiple boards. In this work, Samtec's SEARAY™ family of high-density field array connectors were exploited to achieve these multi-board transitions. This is illustrated in Figure 5. The differential traces from the connector are routed onto the internal layers to minimise losses due to radiation and to minimise crosstalk between channels. The transitions to the internal layers are achieved using differential thru via and micro via structures. These differential via transitions form part of the connector-to-board launch and hence, careful design of the region is required to minimise the effect of discontinuity and to preserve signal integrity.

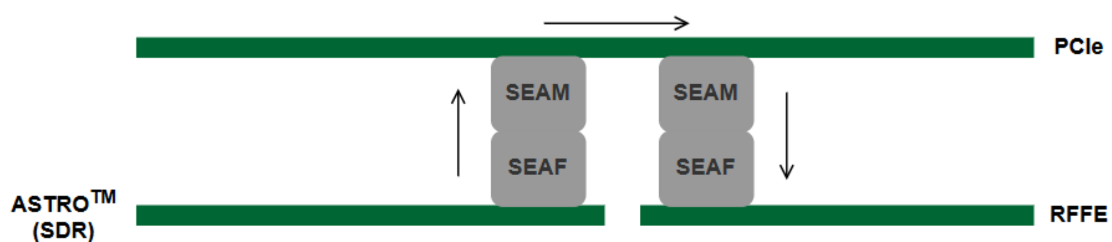


Figure 5 An illustration of multi-board connections using Samtec's SEARAY™ connectors.

The work done to design a test board for evaluation of this connector assembly is described in this paper. A SEAM-SEAF connector assembly with an 11 mm stack-up height was simulated in Ansys HFSS using a 3D component model obtained from the vendor. Differential thru via and microvia structures were simulated separately and then incorporated with the connector pads to design an optimised PCB launch for the chosen PCB stack-up. The two models were simulated together to obtain the complete board-to-board performance. The target specifications are outlined in Table 1 below:

Table 1 Target specifications for connector-to-board transition

Maximum frequency of interest	6 GHz
Target impedance for the differential traces	100 Ω
Worst-case return loss	-20 dB
Maximum insertion loss	-0.5 dB
Crosstalk between channels	-60 dBc

The PCB stack-up and via definitions for the test board are presented in Figure 6 and Figure 7. Microvias were used in this design to achieve the desired high-density interconnections. Microvias are laser-drilled vias, typically of a smaller size than a thru hole via, that are used to connect adjacent layers in a PCB. Vertically aligned microvias are called stacked microvias and have been exploited in this work, as illustrated in Figure 7. A finished thru hole via the size of 0.15 mm diameter with a pad size of 0.50 mm and a 0.15 mm diameter microvia with a 0.30 mm pad size were utilised in the design. Microvias were copper-filled, whereas the plated thru hole vias were resin-filled. Isola I-Tera MT40 was used as the substrate of choice as it is an FR4-based prepreg that is compatible with multi-layer processes. In addition, it has a well-controlled dielectric constant and low loss tangent making it suitable for RF applications.

#	Name	Material	Type	Weight	Thickness	Dk	Df
	Top Overlay		Overlay				
	Top Solder	Solder Resist	Solder Mask		0.02mm	4.1	
1	Top Layer		Signal	1oz	0.037mm		
	Dielectric 1	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
	Dielectric 2	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
2	L02_SIG/GND		Signal	1oz	0.037mm		
	Dielectric 3	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
	Dielectric 4	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
3	L03_SIG/GND		Signal	1/2oz	0.0175mm		
	Dielectric 5	I-Tera MT40 2X2116&3313	Core		0.45mm	3.45	0.02
	Dielectric 6	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
	Dielectric 7	I-Tera MT40 2X2116&3313	Core		0.45mm	3.45	0.02
4	L04_SIG/GND		Signal	1/2oz	0.0175mm		
	Dielectric 8	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
	Dielectric 9	I-Tera MT40 1035 RC73%	Prepreg		0.056mm	3.14	0.02
5	L05_SIG/GND		Signal	1oz	0.037mm		
	Dielectric 10	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
	Dielectric 11	I-Tera MT40 1035 RC73%	Prepreg		0.059mm	3.14	0.02
6	Bottom Layer		Signal	1oz	0.037mm		
	Bottom Solder	Solder Resist	Solder Mask		0.02mm	4.1	
	Bottom Overlay		Overlay				

Figure 6 6-layer PCB stackup for the test PCB

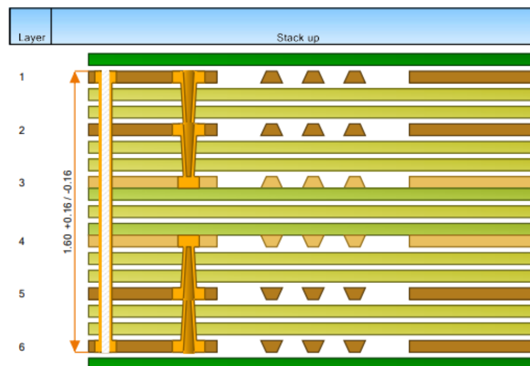


Figure 7 Via definitions for the test PCB. Thru hole plated via and stacked microvias used in the design.

3.1 RF Via Transitions

3.1.1 Thru Differential Vias:

A GSSG (Ground-Signal-Signal-Ground) differential thru via model, transitioning from the Top Layer to Layer 5, was implemented in Ansys HFSS, as shown in Figure 8. Parametric simulations of via spacings were performed and an optimal solution was chosen based on the return loss and TDR (Time-Domain Reflectometry) performance.

Any redundant signal via pads were removed as they introduced unwanted capacitance between pads on adjacent layers. The anti-pads (or clearances) of the two individual vias are combined to form an oval anti-pad on the internal layers, thus, reducing the parasitic capacitance to the ground. The unused length of the via (from Layer 5 to the Bottom Layer) forms a via stub. A via stub has the effect of reducing the bandwidth by introducing a resonance at a frequency where the stub length equals $\lambda/4$. The thru via stub can be eliminated or reduced by a process called backdrilling in which the via stub is drilled away during the PCB fabrication process. However, this comes at an increased cost. In this design, the via stub is 0.118 mm in length, i.e., the theoretical resonant frequency of the stub is > 100 GHz. Hence, backdrilling is avoided at the expense of acceptable performance degradation.

The effect of via spacing on the differential via impedance can be observed in the TDR plot shown in Figure 9 and the corresponding return loss is displayed in Figure 10. Reducing the via spacing increases the capacitive effect of the discontinuity as the mutual capacitance or electric field density between the two vias increases. Similarly, increasing the via spacing increases the inductive effect of the discontinuity. It is evident from Figure 13 that by choosing the appropriate via spacing, a simulated return loss of better than 45 dB and an insertion loss of less than -0.03, up to 6 GHz, can be achieved.

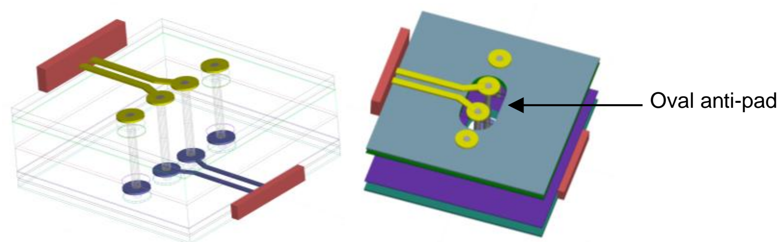


Figure 8 A 3D EM model of a thru via differential GSSG structure

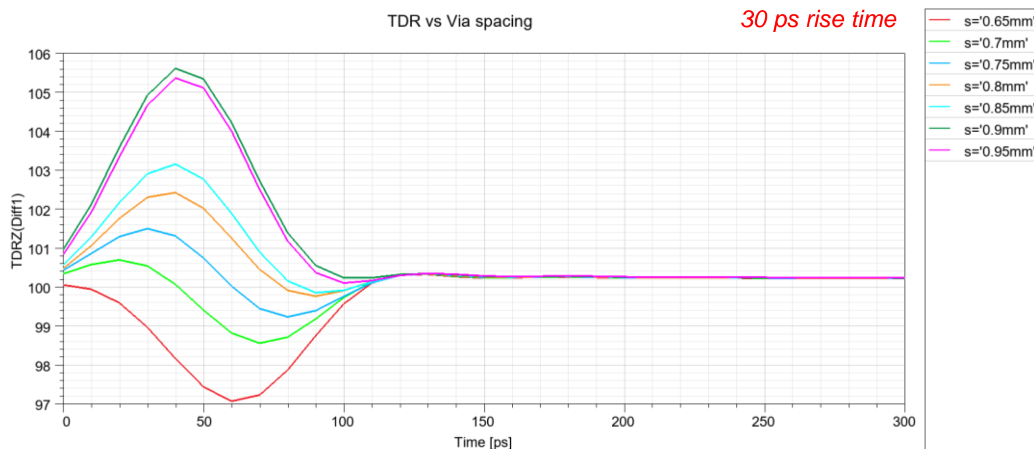


Figure 9 TDR response for parametric simulation of a thru via differential structure for different via spacings.

The connector launch must incorporate the connector pin pads, which are 0.64 mm in diameter and a pitch of 1.27 mm. Incorporating these pads with the differential via transitions has the effect of introducing additional capacitance to the launch area. Hence, a more inductively coupled via spacing is chosen for the connector launch to compensate for the additional capacitance of the connector pads. A thru via spacing of 0.85 mm was chosen as a starting point for the connector launch design.

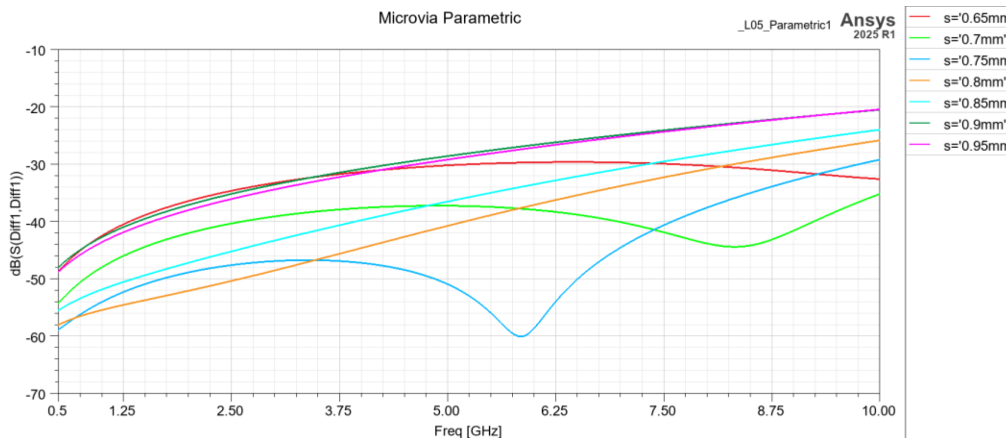


Figure 10 Differential return loss response of a differential thru via structure for different via spacings.

3.1.2 Stacked Microvia Transitions

Stacked microvias improve electrical performance by eliminating via stubs and improving space efficiency. However, this comes at the expense of increased manufacturing costs as incorporation of microvias in the design implies additional manufacturing processes. Microvias are less inductive than plated thru vias as they are much shorter and are copper filled. In addition, the via pad size is much smaller meaning that the capacitance introduced by pads on adjacent layers is lower. Therefore, the overall discontinuity effect of a microvia is much smaller than that of a thru via. Figure 11 shows the 3D EM model of a differential microvia pair between a thru ground via pair.

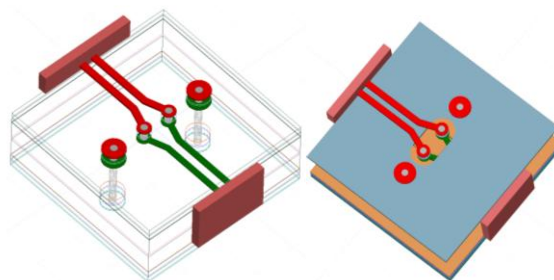


Figure 11 A 3D EM model of a differential microvia GSSG structure

The TDR and return loss performance for different microvia spacings is presented in Figure 12 and Figure ***13***. A comparison of Figure 9 with Figure 12 and that of Figure 10 with Figure 12 shows that in general, the performance of microvias is better than thru vias over a wider bandwidth. A via spacing of 0.80 mm is chosen for the connector launch area with the knowledge that capacitive connector pads will be introduced to the launch design

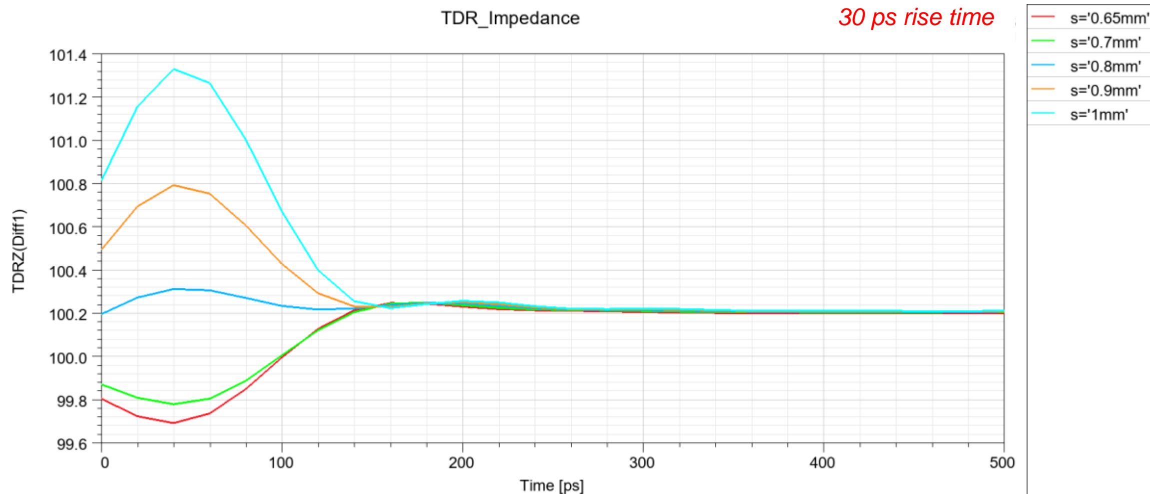


Figure 12 TDR response of a differential microvia via structure for different via spacings

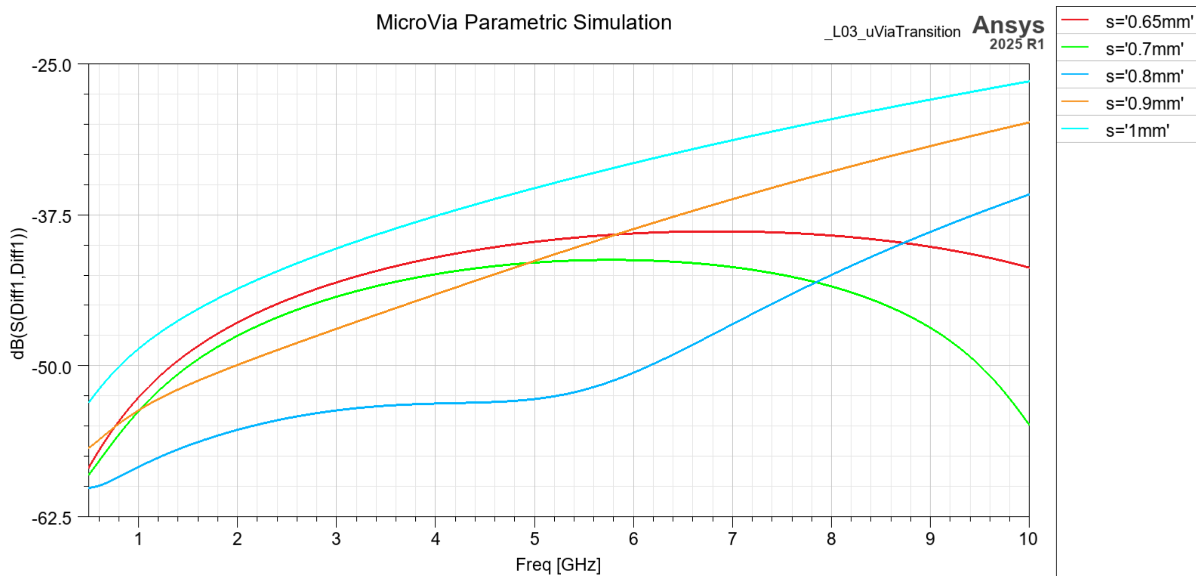


Figure 13 Differential return loss response of a differential thru via structure for different via spacings

3.2 Multi-board connectivity through high-density array connectors

The results from the parametric simulations above provide a starting point for the design of an optimal PCB launch.

3.2.1 Optimal PCB launch with a Thru Via Transition

The 3D model of an optimal connector launch with a thru via transition and its simulated S-parameters are presented in Figure 14. The differential thru vias are pulled into the connector pads whilst maintaining the via spacing identified through the parametric simulations. Ground-plane cutouts under the connector pad are incorporated to increase the distance to the reference ground plane, thereby reducing the capacitive effect of the pads. A ground fence combination of thru and stacked microvias is implemented to reduce crosstalk and improve signal integrity. The launch area was optimised to achieve better than 30 dB return loss and less than 0.04 dB insertion loss up to 6 GHz.

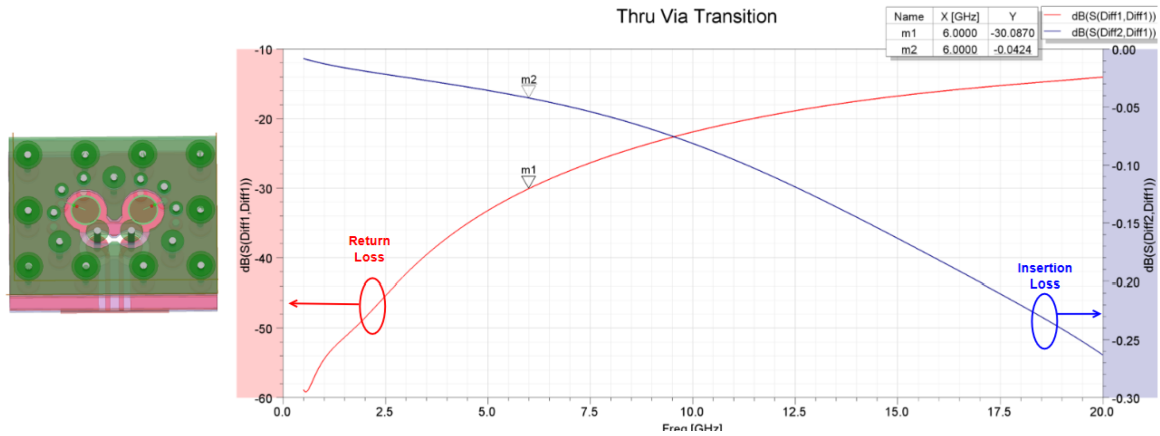


Figure 14 S-parameters for an optimised PCB breakout region with thru via

3.2.2 Optimal PCB launch with a Microvia Transition

The S-parameters for an optimised launch employing a differential microvia structure is presented in Figure 15. As with the thru vias, the microvias are pulled into the connector pads and ground plane cutouts are incorporated under the connector pads on Layer 2. As the differential signal traces are routed on Layer 3, care had to be taken to ensure that no signal passes underneath the ground plane cutout, ensuring the top and bottom reference planes are continuous. The PCB launch was optimised to achieve better than 30 dB return loss and less than 0.04 dB insertion loss up to 6 GHz.

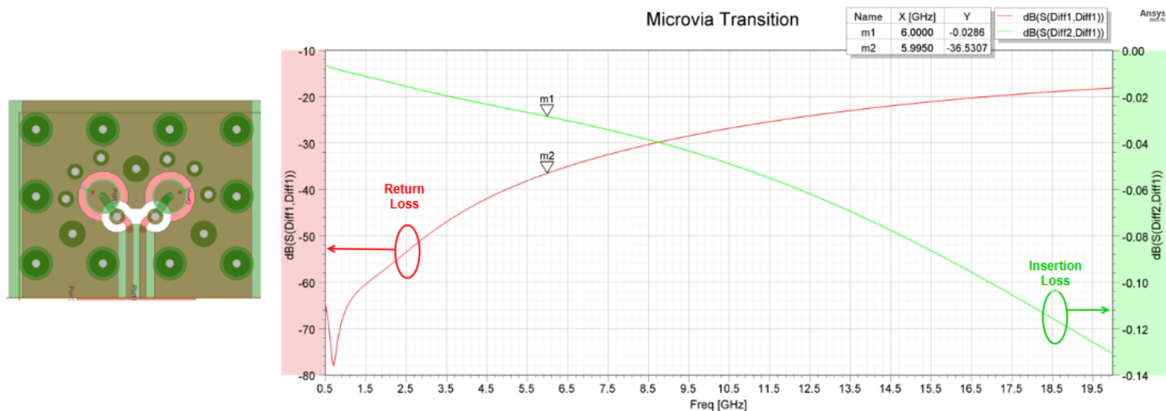


Figure 15 S-parameters for an optimised PCB breakout region with microvia

3.2.3 SEARAY™ Connector Stack-up Simulation

Figure 16 demonstrates an Ansys HFSS 3D component model of Samtec's SEARAY™ connector stack-up with 8 rows and 10 columns. The connector stack-up was simulated in isolation to determine the pin mapping required to achieve the desired inter-channel isolation. The differential signal pairs were arranged along the column to achieve edge coupling versus to broadside coupling as initial simulations indicated that edge coupling configuration provided better return loss performance. The concept of edge coupling and broadside coupling [3] is illustrated in Figure 17. The connector pin mapping was assigned to investigate the crosstalk performance achieved with

two versus four ground pins between two differential signal pairs. The higher the number of ground pins between any two signal pin pairs, the better the crosstalk performance. However, this is at the expense of a larger connector size and consequently, more PCB real estate. Worst case return loss of -17 dB and maximum insertion loss of -0.27 dB is observed at 6 GHz. The return loss of the SEAF is approximately 1.8 dB worse than that of its SEAM counterpart, potentially due to the longer pin lengths of the SEAF connector. It is favourable to reduce the connector stack height as a larger stack height implies more insertion loss and higher crosstalk.

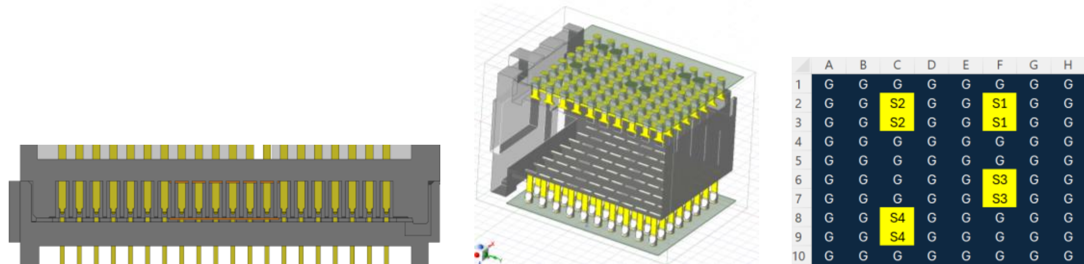


Figure 16 Mated view of the SEAX assembly, an encrypted 3D EM model of the SEAX connector assembly and the corresponding pin-mapping. Signal pairs are indexed based on their port names in the simulation. The connector terminal indices for the simulation are as identified in the pin mapping above.

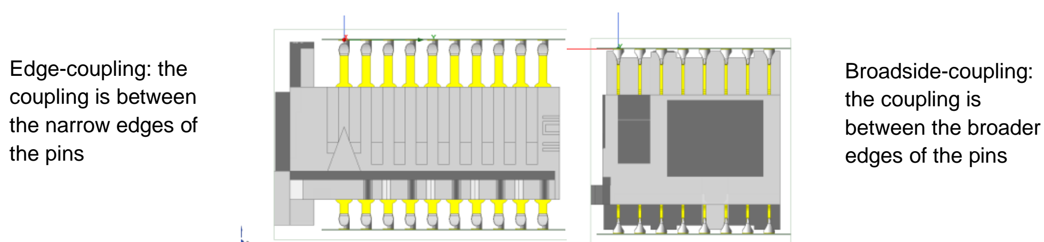
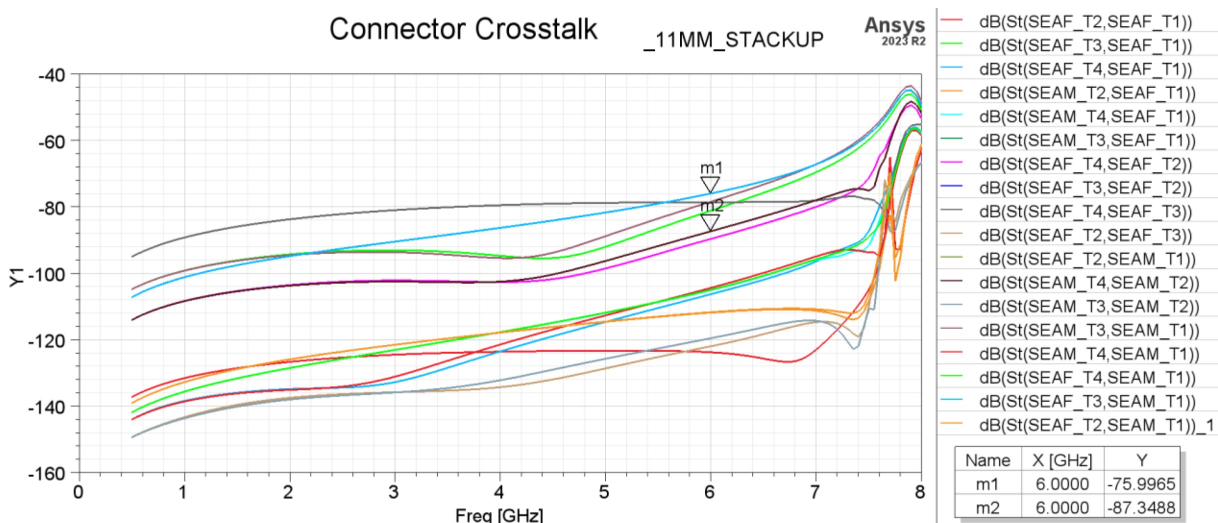


Figure 17 Edge-coupling vs. Broadside coupling of the SEARAY™ connector pins

The connector crosstalk performance for the chosen pin mapping is displayed in Figure 18. Increasing the ground pin pairs from 2 to 4 improves the inter-channel isolation by approximately 11.5 dB. It must, however, be noted that as the number of aggressor channels (other signal pairs) around a victim channel is increased, the crosstalk observed will degrade.



Name	X [GHz]	Y
m1	6.0000	-75.9965
m2	6.0000	-87.3488

Figure 18 Simulated crosstalk performance of the SEAX connector assembly.

The crosstalk for board-to-board simulation is displayed below. It is evident that the crosstalk performance is similar to the connector crosstalk performance, implying that the pin mapping through the connector is dominating the crosstalk performance achieved. It must be noted that these connectors are typically intended to be used in digital applications where crosstalk is not a key specification parameter.

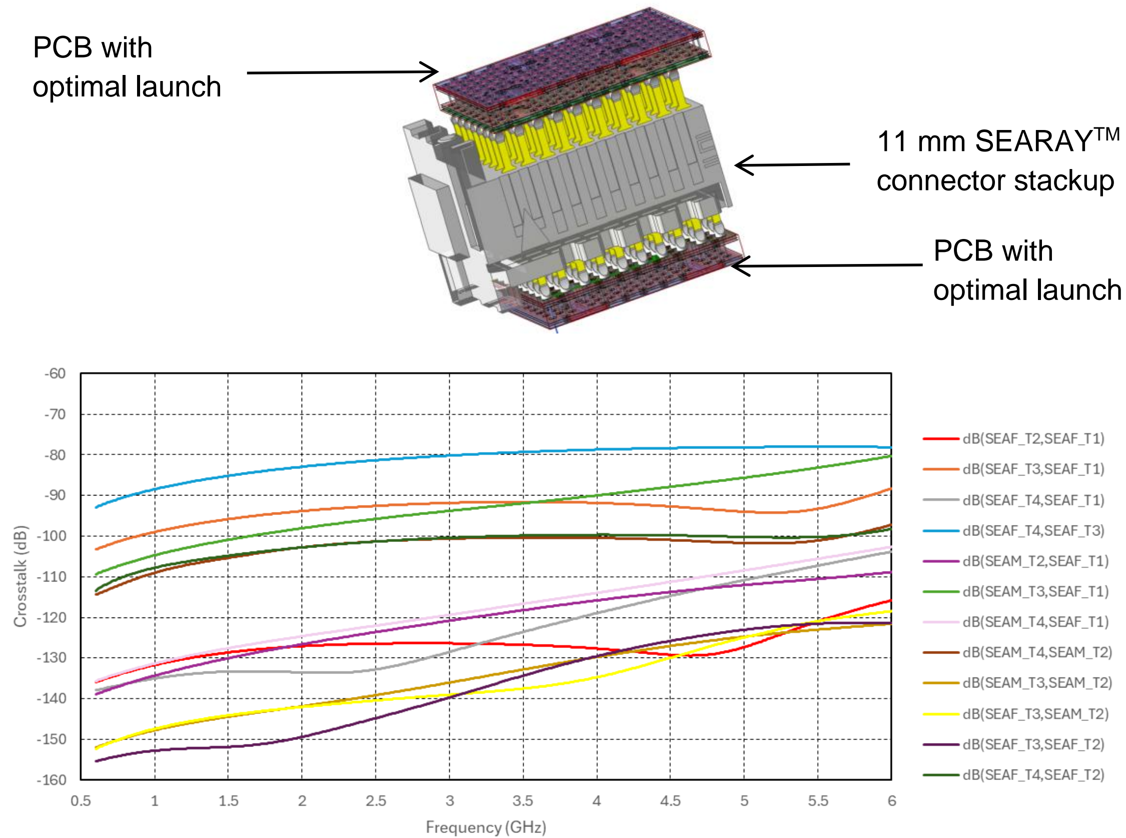


Figure 19 A 3D EM model of the SEARAY™ connector assembly between two PCBs and the corresponding crosstalk simulation. The connector terminals are defined in the pin mapping in Figure 16.

4. Summary

The design challenges in realising a compact multi-board RFSoC-based SDR platform have been discussed with a key focus on HDI implementation. High-density array connectors, which are intended for digital applications, have been utilised for achieving analogue RF interconnections by means of careful design. The critical role of pin mapping of this connector in achieving high inter-channel isolation (> 60 dBc) for RF applications has been highlighted. Simulation results, up to 6 GHz, for connector-to-board transitions and complete board-to-board transitions have been presented.

The next step includes extending the presented work to 18 GHz to enable evaluation of the connector for AMD's incoming Versal Adaptive SoC device. Custom test PCBs, based upon above simulations, are to be fabricated and measured to assess the suitability of the connectors and verify the simulations up to 18 GHz.

5. References

[1]TRP-C16648-ARMMS-Paper-April-2024-Generation-of-Complex-Waveforms-through-the-Development-of-a-Wideband-Digitally-Controlled-Power-Amplifier-P030-0-CICV2.0.pdf

[2] Overview • Zynq UltraScale+ RFSoC RF Data Converter v2.6 Gen 1/2/3/DFE LogiCORE IP Product Guide (PG269) • Reader • AMD Technical Information Portal

[3] samtec-array-connectors-for-mixed-sigal-multi-channel-rfsocs.pdf